SEMICONDUCTOR STRUCTURE HAVING STRAINED SEMICONDUCTOR AND METHOD THEREFOR

Field of the Invention

This invention relates to semiconductor devices, and more particularly, to semiconductor devices that are made in active area of semiconductor that is strained.

Related Art

A continuing desire for transistors is that they have improved performance. One of these importance performance characteristics is the current that the transistor can carry for a given input, which is based on the carrier mobility. This is often referenced as the I V curve, which is the curve that is a plot of drain current versus gate to source voltage. This electron and hole mobility is desirably increased but also it is important to keep leakage low.

Thus, there is a need for improved carrier mobility for transistors while maintaining low leakage.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 is a cross section of a first semiconductor structure useful in a first embodiment of the invention;

FIG. 2 is a cross section of a second semiconductor structure useful to the first embodiment of the invention; and

FIG. 3 is a cross section of a third semiconductor structure that combines the first and second semiconductor structures according to the first embodiment of the invention;

FIG. 4 is a cross section of the third semiconductor structure of FIG. 3 at a subsequent stage in processing according to the first embodiment of the invention;

FIG. 5 is a cross section of the third semiconductor structure of FIG. 4 at a subsequent stage in processing according to the first embodiment of the invention;

FIG. 6 is a cross section of the third semiconductor structure of FIG. 5 at a subsequent stage in processing according to the first embodiment of the invention; and

FIG. 7 is a top view of the first and second semiconductor structures of FIG. 6 being combined according to the first embodiment of the invention.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

In one aspect active semiconductor is achieved by combing a first semiconductor structure and a second semiconductor structure. The first semiconductor structure has a base of silicon, a first silicon germanium layer grown on the silicon that is a transition layer, a second silicon germanium layer on the first silicon germanium layer that is substantially monocrystalline and less defective compared to the first silicon germanium layer. The second semiconductor structure has a base of silicon and a top layer that is an insulator layer. The silicon layer of the first semiconductor structure is bonded to the insulator layer to form a third semiconductor structure. The second silicon germanium layer is cut to separate most of the first semiconductor structure from the third semiconductor structure. The silicon germanium layer is removed to expose the silicon layer, and transistors are formed in the silicon layer, which is then the only layer remaining from the first semiconductor structure. The transistors are oriented along the <100> direction and at substantially a 45 degree angle to the <110> direction of the base silicon layer of the second silicon. This is better understood by reference to the figures and the following description.

Shown in FIG. 1 is a semiconductor structure 10 comprising a semiconductor layer 12 of silicon, a silicon germanium layer 14 on semiconductor layer 12, a silicon germanium layer 16 on silicon germanium layer 14, and a silicon layer 18 on silicon germanium layer 16. In this cross section the <100> direction of the crystal of silicon layer 12 is laterally along the face of the cross section. The angle brackets (< >) indicate a family of directions; in this case 100, 010, and 001. Silicon layer 18 preferably has a top surface having an orientation of {100}. This top surface of silicon layer 18 may alternatively have the {110} orientation. The braces ({}) indicate a family of planes. For example, in the case of {100} it means the 100, 010, and 001 planes.

Silicon layer 12 is much thicker than any of the other layers and may be around 500 microns. Silicon layer 12 is useful in providing structural support. Silicon germanium layer 14 is made by providing silicon and adding germanium content until a predetermined amount is reached. An effective amount for this predetermined amount of germanium has been found to be 25% germanium. Silicon germanium layer 14 thus has a graded germanium concentration from 0% at the interface with silicon layer 12 to 25% at the interface with silicon germanium layer 16 such that it may be at least partially relaxed. Silicon germanium layer 16 is made using a consistent amount of germanium, which in this case is 25%. Silicon germanium layer 14 is about 2.5 microns in thickness. Silicon germanium layer is about 0.25 microns in thickness. Silicon layer 18 is much thinner at about 200 Angstroms. This structure is readily achieved using well known semiconductor on insulator (SOI) manufacturing techniques. The crystal orientation of silicon layer 12 is transferred to silicon germanium layer 14 but it becomes more relaxed as the silicon germanium grows. Silicon germanium layer 16 is preferably fully relaxed but maintains the same orientation. The resulting silicon layer, grown on silicon germanium layer 16, is strained due to being under tensile stress. A hydrogen or helium implant is performed to form an implant line 20 in silicon germanium layer 16. This implant line 20 creates a region that aids splitting silicon germanium layer 16.

Shown in FIG. 2 is a semiconductor structure 22 having a silicon layer 24 and a buried oxide layer 26. Silicon layer 24 has a crystal lattice in which a direction lateral along the cross section is the <110> direction. This is the direction in which silicon most naturally breaks. Thus it is desirable to break up individual integrated circuits along this direction. A plane along the surface of silicon layer 24 is the {100} orientation. Silicon base layer is about 500 microns in thickness. Buried oxide layer 26 is about 1400 Angstroms.

Shown in FIG. 3 is a semiconductor structure 30 which combines semiconductor structures 10 and 22 by inverting semiconductor structure 10 and bonding silicon layer 18 with buried oxide layer 26. This bond is made by applying heat. Silicon layer 18 will have at least a thin native oxide and it may be desirable to increase that thickness prior to joining semiconductor substrates 10 and 22. The cross section shown in FIG. 3 is the same as that for semiconductors structures 10 and 22 shown in FIGs. 1 and 2. Thus semiconductor structure 30, after the joining has been formed, has silicon layer 24, buried oxide layer 26 on silicon layer 24, silicon layer 18 on buried oxide layer 26, silicon germanium layer 18 on silicon layer 18, silicon germanium layer 14 on silicon germanium layer 16, a silicon layer 12 on silicon germanium layer 14, and implant line 20 in silicon germanium layer 16.

Shown in FIG. 4 is semiconductor structure 30 after splitting silicon germanium layer 16 at implant line 20. This leaves a portion of silicon germanium layer 16 and silicon layer 18 over buried oxide layer. At this point semiconductor structure 30 comprises a semiconductor structure 22, silicon layer 18 on buried oxide 26, and the portion of silicon germanium layer 16 on silicon layer 18. Laterally along the cross section of silicon layer 18 is the <100> direction. Laterally along the cross section of silicon layer 24 is the <110> direction. The plane of the interface between silicon layer 18 and buried oxide layer 26 and the plane of the interface between silicon layer 24 and buried oxide layer 26 is the {100} plane. Because silicon layer 18 is already bonded to buried oxide layer 26 when silicon layer 12 is severed from silicon layer 18, the tensile stress is maintained as is the resulting strain.

Shown in FIG. 5 is semiconductor structure 30 after removal of the remaining portion of silicon germanium layer 16. The result is a semiconductor on insulator (SOI) substrate useful in making transistors. This SOI substrate has

strained silicon for the active area for the transistors and this strained silicon has its <100> direction being the same as silicon layer 24's <110> direction.

Shown in FIG. 6 is semiconductor structure 30, after formation of transistors 32 and 34, formed in and over silicon layer 16 which is a pre-strained silicon layer because it is strained prior to transistor formation including prior to formation of the isolation regions. Transistor 32 has a gate 36 over silicon layer 16, a sidewall spacer 38 around gate 36, a gate dielectric 40 between gate 36 and silicon layer 16, a source/drain region 42 on one side of gate 36 in silicon layer 16, a source drain region 44 on an opposite side of gate 36 in silicon layer 16, and a channel 46 between source/drain regions 42 and 44. Transistor 34 has a gate 48 over silicon layer 16, a sidewall spacer 50 around gate 48, a gate dielectric 52 between gate 48 and silicon layer 16, a source/drain region 54 on one side of gate 48 in silicon layer 16, a source drain region 56 on an opposite side of gate 48 in silicon layer 16, and a channel 58 between source/drain regions 54 and 56. Transistors 32 and 34 are separated by a tunnel isolation 60 formed of an insulator. Transistors 32 and 34 have their source/drains aligned in the <100> direction while having the substrate, silicon layer 24, which by far most strongly influences the direction of breaking of the silicon, be in the <110>. Transistors have active areas of strained silicon, current paths in the <100> direction, and break direction as well along the <100> direction. Thus the benefits of both strained silicon for N channel transistor enhancement and <100> for P channel transistor are obtained while maintaining the ability to break the wafers aligned to the transistor direction. This is an important alignment criteria due to the manner in which lithography equipment operates and layout design is performed. Transistors 32 may both be P or N type or different types of transistors.

Shown in FIG. 7 is the forming of semiconductor structure 30 by combining semiconductor structures 10 and 22. Semiconductor structure 10

comprises a wafer having a notch 62 that is aligned to the <100> direction. Semiconductor structure 22 comprises a wafer having a notch 64 that is aligned to the <110> direction. This shows that notches 62 and 64 are aligned to each other to achieve the desired differing directions of orientation of the two wafers. Also shown in semiconductor structure 10 is transistor 32 and a transistor 51, which has a 90 degree alignment change compared to transistor 32. Transistor 32 has gate 36 in one direction, transistor 51 has a gate 53 in an orthogonal direction to that of the gate of transistor 32. This shows transistor alignments are along the <100> direction, which has been found to have as much as a 50% improvement in the I-V characteristic for small width devices, such as devices with channel widths below 0.5 micron.

As an alternative, an SOI wafer can be made having these similar characteristics by not growing silicon layer 18 on semiconductor structure 10. In such case a silicon germanium layer is in direct contact with the buried oxide layer 26. The severing can be accomplished in the same way so that there is a silicon germanium layer exposed above buried oxide layer 26. A strained silicon layer can then be grown on this silicon germanium layer and transistors formed on the grown strained silicon layer. In this case as well, the transistors are formed aligned to the <100> direction, the integrated circuit is cut from the wafer aligned to the <100> direction of the active semiconductor layer, and direction of the cut is in the <110> direction of the thick silicon that is the substrate. There may be advantages in providing different stresses in this approach and may provide more ability to separately optimize P and N channel transistors.

As another alternative, silicon layer 16 may be transferred from a simpler semiconductor structure than semiconductor structure 10. In such case the silicon is not stressed. This is a common approach for transferring a silicon layer to the buried oxide layer to form an SOI wafer. The difference is that the

silicon layer being transferred that has a {100} phase is transferred such that it's <100> direction is 45 degrees offset from the <100> direction of the underlying thick silicon substrate. As an alternative this silicon layer being transferred can have a {110} phase. After the silicon formation, a germanium condensation process may be used to develop a silicon germanium layer. This is known to be achievable by forming silicon germanium and oxidizing that layer which has the effect of driving germanium into the silicon layer with the desired concentration of germanium. The upper oxide layer is removed leaving a silicon germanium layer that has the desired concentration of germanium. A subsequent layer of silicon is then grown from the silicon germanium layer with the desired germanium concentration. This silicon over silicon germanium then forms the active semiconductor layer for transistor formation and can be made to have the desired strain based on the underlying germanium concentration and with the desired <100> orientation for transistor formation.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, other semiconductor materials different from germanium and silicon may be used in this manner to achieve this result. Various thicknesses have been specified but they can be changed. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to

be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.